Atty. Docket No. PIA31191/ANS/US
Serial No: 10/765,027

Amendments to the Claims

Please cancel claims , add new claims , and amend the remaining claims as follows:

1. (Currently Amended) A method for manufacturing a MOSFET device, the method comprising:

1) ~~selectively~~ forming a shallow trench isolation in a substrate;
2) forming a first oxide layer on a surface of an active region of the substrate and implanting ions thereinto for forming a ~~low~~ lightly doped drain in the active region prior to the formation of a gate;
3) forming a first nitride layer;
4) removing a part of the first nitride layer and the first oxide layer ~~where the gate will be located~~ and etching the substrate corresponding to the part, including the lightly doped drain, by a ~~predetermined~~ depth of about 200 to about 1000 angstroms to define a gate region;
5) forming a second oxide layer over an exposed portion of the substrate;
6) implanting ions into the substrate;
7) removing the second oxide layer;
8) depositing a gate insulating layer and a polysilicon layer into the removed parts of the first nitride layer and the first oxide layer;
9) polishing until the first nitride layer is exposed;
10) removing the first nitride layer, depositing an oxide layer conformally and depositing ~~an~~ a second nitride layer;
11) etching the second nitride layer to form a gate sidewall ~~of nitride~~;
12) implanting ions into the substrate to form a source and drain at ~~both~~ sides of the gate; and
13) removing an exposed oxide layer.

2. (Original) A method as defined by claim 1, wherein the substrate comprises a silicon substrate.

3. (Original) A method as defined by claim 1, wherein the shallow trench isolation comprises an oxide layer.

4. (Canceled)

5. (Original) A method as defined by claim 1, wherein forming the second oxide layer comprises oxidizing the exposed substrate ~~is oxidized~~ at a temperature of from about 600 to about 800 °C, such that ~~to form~~ the second oxide layer ~~having~~ has a thickness of about 100 angstroms ~~in (e)~~.

6. (Original) A method as defined by claim 1, wherein a the polishing comprises chemical mechanical polishing ~~is performed in (i)~~.

7. (Currently Amended) A method as defined by claim 1, wherein removing the second nitride layer ~~is removed by an~~ comprises etch back processing ~~in (k)~~.

8. (New) A method for manufacturing a MOSFET device, the method comprising:
   1) implanting ions into an active region of a substrate to form a lightly doped drain (LDD) prior to forming a gate;
   2) forming a first nitride layer on the substrate, including the active region;
   3) removing part of the first nitride layer and etching the exposed substrate, including the LDD, to a predetermined depth to define a gate region;
   4) implanting ions into the substrate to control a voltage threshold of the MOSFET device;
   5) forming a gate insulating layer and a polysilicon layer in the gate region;
   6) removing the first nitride layer, then depositing an oxide layer and a second nitride layer on the polysilicon layer;

7) etching the second nitride layer to form a gate sidewall; and

8) implanting ions into the substrate to form a source and drain at sides of the gate.

9. (New) A method as defined by claim 8, wherein the substrate comprises a silicon substrate.

10. (New) A method as defined by claim 8, further comprising forming a shallow trench isolation in the substrate to define the active region prior to implanting ions to form a LDD.

11. (New) A method as defined by claim 10, wherein the shallow trench isolation comprises an oxide layer.

12. (New) A method as defined by claim 8, wherein forming the second oxide layer comprises oxidizing the exposed substrate at a temperature of from about 600 to about 800 °C, such that the second oxide layer has a thickness of about 100 angstroms.

13. (New) A method as defined by claim 8, wherein forming the polysilicon layer comprises depositing polysilicon onto the gate insulating layer in the gate region and chemical mechanical polishing the polysilicon.

14. (New) A method as defined by claim 13, wherein forming the gate insulating layer comprises depositing the gate insulating layer in the gate region.

15. (New) A method as defined by claim 8, wherein removing the second nitride layer comprises etch back processing.

16. (New) A method as defined by claim 8, wherein the predetermined depth is from about 200 to about 1000 angstroms.

17. (New) A method as defined by claim 8, further comprising, prior to implanting ions into the substrate to control the voltage threshold of the MOSFET device, forming a second oxide layer over an exposed portion of the substrate.

18. (New) A method as defined by claim 17, further comprising, after implanting ions into the substrate to control the voltage threshold of the MOSFET device, removing the second oxide layer.

19. (New) A method as defined by claim 8, further comprising, after implanting ions into the substrate to form the source and drain, removing an exposed oxide layer.